WHAT IS CLAIMED IS:

1. A method for programming a memory device having a programming node, comprising:

providing a programming voltage to the programming node;

using the programming voltage to generate a load current;

generating a load voltage at a compensation node of the memory device;

generating an error voltage in response to the load voltage; and

changing the load current in response to the error voltage.

2. The method of claim 1, wherein generating the error voltage includes comparing a reference voltage with the load voltage.

3. The method of claim 2, wherein the error voltage increases the load current when the reference voltage has a greater value than the load voltage.

4. The method of claim 1, wherein changing the load current further includes providing an enable signal at a switching terminal.

5. The method of claim 1, wherein providing the programming voltage includes providing the programming voltage to a plurality of programming nodes.

6. The method of claim 5, wherein providing the programming voltage includes providing the programming voltage to sixteen programming nodes.

7. The method of claim 1, wherein changing the load current includes increasing the load current.

8. A method for regulating a programming voltage in a memory device, comprising:

generating a load current in accordance with the programming voltage; and

changing the load current in response to a programming load by applying the programming voltage to a load compensation network, wherein the load compensation network changes the load current to simulate programming a predetermined number of data bits of the memory device.

9. The method of claim 8, wherein generating the load current further includes generating a load current in accordance with the number of data bits being programmed.

10. The method of claim 9, wherein the number of data bits being programmed is sixteen.

11. The method of claim 8, wherein the predetermined number of data bits is sixteen.

12. The method of claim 8, wherein changing the load current includes generating a load compensation current through a programming load.

13. The method of claim 8, wherein changing the load current includes:

comparing a compensation voltage signal with a reference voltage signal to generate an error voltage signal;

generating an output voltage signal in accordance with the error voltage signal; and

using the output voltage signal to change the load current.

14. The method of claim 13, wherein using the output voltage signal to change the load current includes activating a transistor.

15. A memory device, comprising:

a programming circuit having an input terminal and a programming terminal, the programming terminal coupled for receiving a programming signal; and

a load current compensation circuit having a control terminal and an input terminal coupled for receiving the programming signal.

16. The memory device of claim 15, wherein the load current compensation circuit comprises:

a first switching element having a control electrode and first and second current conducting electrodes; and

a load element having first and second terminals, the first terminal coupled to the first current conducting electrode of the switching element and the second terminal coupled to a source of operating potential.

17. The memory device of claim 16, wherein the load current compensation circuit further comprises a differential amplifier having first and second input terminals, an enable input terminal, and an output terminal, the first input terminal coupled to the second current conducting electrode of the switching element and the output terminal coupled to the control electrode of the first switching element.

18. The memory device of claim 17, wherein the first and second input terminals cooperate to form a differential input.

19. The memory device of claim 18, wherein the second input terminal of the differential amplifier is coupled for receiving a reference signal.

20. The memory device of claim 19, wherein the load current compensation circuit further includes a switching network having a pair of differential input terminals, a control terminal and first and second bias terminals, the control terminal and the first bias terminal coupled for receiving the programming signal and the second bias terminal coupled to the first current conducting electrode of the first switching element.

21. The memory device of claim 16, wherein the load current compensation circuit further includes a second switching element having a control terminal and first and second bias terminals, the first bias terminal coupled for receiving the programming

signal and the second bias terminal coupled to the first current conducting electrode of the first switching element.